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Peter J. Yim
Morrison & Foerster LLP
425 Market Street
San Francisco, CA 95148

EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,172	NGUYEN ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-20* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/2002*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1. Original claims 1-20 are pending.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "distributes" on line 2 is interpreted as "distribute". Appropriate correction is required.

3. Claim 16 is objected to because of the following informalities: "integrated circuit" on line 2 is interpreted as "PLD". Appropriate correction is required.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 10, 11, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al., U.S. Patent No. 6,191,609 ("Chan").

As per claim 1, Chan discloses a clock network for an integrated circuit (col. 1, lines 11-15) comprising:

a first set of lines configured to distribute clock signals to a first section of the integrated circuit (fig. 2, localized clock structure 44 in upper left quadrant with lines 58);

a second set of lines configured to distribute clock signals to a second section of the integrated circuit separately from the first section of the integrated circuit (fig. 2, localized clock structure 44 in lower left quadrant with lines 58); and

a third set of lines configured to distribute clock signals to both the first and second sections of the integrated circuit (fig. 2, global clock structure 42 with line 48, lines 52 and lines 54).

As per claim 10, Chan discloses a clock network for a programmable logic device (PLD), wherein the PLD includes a first set of logic resources and at least a second set of logic resources (fig. 2, programmable logic device 40 includes cells 60 in upper left quadrant and in lower left quadrant), the clock network comprising:

a first set of clock lines configured to distribute clock signals to the first set of logic resources separately from the second set of logic resources (fig. 2, localized clock structure 44 in upper left quadrant with lines 58; col. 5, lines 3-7; col. 4, lines 4-10); and

a second set of clock lines configured to distribute clock signals to the second set of logic resources separately from the first set of logic resources (fig. 2, localized clock structure 44 in lower left quadrant with lines 58).

As per claim 11, Chan discloses a third set of clock lines configured to distribute clock signals to both the first and second sets of logic resources (fig. 2, global clock structure 42 with line 48, lines 52 and lines 54; col. 5, lines 3-7; col. 4, lines 4-10).

As per claim 17, Chan discloses a method for distributing clock signals within an integrated circuit (col. 1, lines 11-15) using a clock network comprising:

distributing clock signals to a first section of the integrated circuit using a first set of lines of the clock network (fig. 2, localized clock structure 44 in upper left quadrant with lines 58); and

distributing clock signals to a second section of the integrated circuit separately from the first section using a second set of lines of the clock network (fig. 2, localized clock structure 44 in lower left quadrant with lines 58).

As per claim 18, Chan discloses distributing clock signals to both the first and second sections of the integrated circuit through a third set of lines of the clock network (fig. 2, global clock structure 42 with line 48, lines 52 and lines 54).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-8, 12-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan as applied to claims 1, 11 and 17 above, and further in view of Duong et al., U.S. Patent No. 5,172,579 ("Duong").

As per claim 2, although Chan teaches driving logic resources with both global and local clock lines and that connections exist between the three sets of clock lines and corresponding logic resources (col. 4, lines 4-10), Chan does not expressly teach details of lines disposed in the first and second sections. Duong teaches first and second sections of an integrated circuit (fig. 3, quadrants 5 and 9 of FPGA 100), further comprising:

at least one line disposed in the first section that connects to the first and third sets of lines (fig. 4A, channel 221a connects to two sets of clock lines via mux 210; col. 4, line 46 – col. 5, line 3; col. 5, lines 37-59); and

at least one line disposed in the second section that connects to the second and third sets of lines (fig. 4A, channel 221c connects to two sets of clock lines via mux 214; col. 5, lines 9-30).

Chan teaches further providing more than one clock source (col. 3, lines 24-33). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Duong's means for connecting between a line, disposed in a section, to two sets of clocks lines to Chan's clock network, in order to permit flexibility in selecting a clock source.

As per claim 3, Duong teaches the first and third sets of lines converge at the center of the first section (fig. 4A, sets of lines converge at mux 210), and wherein the second and third sets of lines converge at the center of the second section (fig. 4A, sets of lines converge at mux 214).

As per claim 4, Duong teaches the at least one line disposed in the first section is connected directly to an input/output (I/O) of the integrated circuit to receive an input-clock signal (col. 5, lines 42-50 & 60-65).

As per claim 5, Duong teaches the integrated circuit includes a plurality of logic resources, wherein the at least one line in the first section connects to the plurality of logic resources in the first section (col. 5, lines 4-8; col. 3, lines 62-66), and wherein the at least one line in the second section connects to the plurality of logic resources in the second section (col. 5, lines 31-36; col. 3, lines 62-66).

As per claim 6, Duong teaches the integrated circuit includes a plurality of logic resources, and wherein the third set of lines is configured to receive an input-clock signal from at least one logic resource (fig. 4A; col. 5, lines 42-50; col. 5, lines 60 – col. 6, lines 4).

As per claim 7, Duong teaches the third set of lines is connected to a sneak path from the at least one logic resource (fig. 4A; col. 5, lines 60 – col. 6, lines 4).

As per claim 8, Duong teaches the third set of lines is configured to receive an input-clock signal from a dedicated input-clock pin (fig. 4A; col. 5, lines 42-50; col. 5, lines 60 – col. 6, lines 4).

As per claims 12-15, since Chan/Duong teaches the clock network of claims 2-8 and the clock network of claim 11, the combination teaches the claimed clock network.

As per claim 19, since Chan/Duong teaches the clock network of claims 2-8 and the method of claim 17, the combination teaches the claimed method.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan/Duong, as applied to claim 15 above, and further in view of Hull et al., U.S. Patent No. 5,686,844 ("Hull").

As per claim 16, Chan/Duong does not expressly teach the first and second signal lines receive input-clock signals from input pins of the integrated circuit that are not dedicated as input-clock pins. Hull teaches an integrated circuit pin that is configurable either as a clock input pin or as a digital I/O pin (fig. 1; col. 3, lines 7-42). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Hull's configurable pin to Chan/Duong's PLD. A motivation for doing so would have been to increase the flexibility of the PLD (Hull, col. 1, lines 27-39).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan, as applied to claim 17 above, and further in view of Hull et al., U.S. Patent No. 5,686,844 ("Hull").

As per claim 20, Chan/Duong does not expressly teach the first and second signal lines receive input-clock signals from input pins of the integrated circuit that are not dedicated as input-clock pins. Hull teaches an integrated circuit pin that is configurable either as a clock input pin or as a digital I/O pin (fig. 1; col. 3, lines 7-42). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Hull's configurable pin to Chan/Duong's integrated circuit. A motivation for doing so would have been to increase the flexibility of the integrated circuit (Hull, col. 1, lines 27-39).

Allowable Subject Matter

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
February 22, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100